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DESIGN AND DEVELOPMENT OF 51 LEVEL NON MODULAR MULTILEVEL INVERTER TOPOLOGY WITH REDUCED NUMBER OF SWITCHES AND CONDUCTION PATH

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ABSTRACT

In this paper, a 51 level multilevel inverter topology with non modular design is developed, which can be operated in asymmetrical mode with a reduced number of power switches and lesser conduction path. The proposed design has three separated DC sources and eleven active power switches, i.e., ten unidirectional switch and one bidirectional switch. The topology can be used with asymmetrical voltage source configuration to generate fifty one levels. This structure can be cascaded to produce maximum level by a series connection to produce higher voltage levels with less voltage stress on the switches without modifying the topology structure. A detailed Comparison is made with existing topology and recently introduced topologies based on the number of active switches, Separated DC sources, number of gate driver circuits. To prove the presented topology's superiority, a simple Multicarrier pulse width modulation has been deployed as the switching scheme. Validation on the viability of the proposed topology has been carried out through Matlab/Simulink simulation.

KEYWORDS: *Non Modular Multilevel Inverter, Reduced Switch.*

I. INTRODUCTION

The MLIs is same as the to conventional two level inverters (TLIs) but the MLI can able to produces maximum number of stair case wave form in the output and also has the following merits like lower dv/dt and lesser switching device stress, a minimized output distortion, reduced switching losses, a minimal EMI losses (EMI), the introduction of MLI is emerging last four decades, which is existence in the year 1975, many topologies have been developed by various researchers, which are comprised with many obstacles etc. The multilevel inverter (MLI) is basically a voltage source inverter (VSI), which has good ac output voltage wave form in stair case with the rated frequency of 50Hz or 60Hz from single or group of separate dc sources (SDCs) . A new pulse width modulation strategy is proposed for the multilevel inverter with switching per modulation cycle at each level in MLI which is dependent carrier frequency [1].

A new 8-level basic structure for cascaded multilevel inverters is developed with basic structure, two different cascaded multilevel topologies are proposed. The presented cascaded multilevel inverters use less number of power switches, IGBTs and dc voltage sources compared with the conventional multilevel inverters [2]. A new single-phase cascaded multilevel inverter with a series connection in the basic unit and is able to only generate positive levels at the output. The reduction in switching device and driver circuit is added advantage [3]. A new tapped source stack succored modified HX Bridge MLI topology is developed, which has tapped sources stack (TSS) and modified HX bridge inverter, the systems is implemented with the multicarrier/sub-harmonic pulse width modulation scheme [4]. A new MLI structure called a flexible rung ladder structured multilevel inverter (FRLSMLI), with a savvy to operate both in symmetrical and asymmetrical modes involving only fewer component counts. The FRLSMLI is basically a

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ladder structured bridge (H-bridge with additional rungs) and the rungs comprise either source inclusion-bypass cell (SIBC) or four level creator cells [5]. A two-stage switched-capacitor based multilevel inverter has drawback such that switches in the second stage is affected with higher voltage stress. To overcome this problem, a single-stage switched-capacitor module topology for cascaded multilevel inverter is proposed [6]. An ingenious symmetrical MLI topology, which consumes lesser component count is proposed with level dependent sources concoction multilevel inverter (LDSCMLI) is basically a multilevel dc link MLI (MLDCMLI), which first synthesizes a stepped dc link voltage using a sources concoction module and then realizes the ac waveform through a conventional H-bridge [7]. A non modular matrix structure MLI topology is deployed with reduced switch count. The idea of the modified matrix structure MLI (MMSMLI) is involving switches in columns and separate DC sources (SDCs) in the row links, through which the addition and subtraction amid the SDCs are made easy in the asymmetrical operation, and hence the creation of more output levels are possible [8]. Modeling of cascaded multilevel inverter (MLI) for harmonics mitigation of induction motor is proposed. Three-phase five- and seven-level inverters are developed with reduced THD [9]. A new switching scheme is developed for the cascaded multilevel inverter with PI and FLC controller to produce nine level at the output with lesser THD [10]. Performance analysis of modular and non modular multilevel inverter in various aspects like, topology design, input voltage i.e. symmetric or asymmetric, objectionable components count reduction, modulation index (m), stair case voltage levels, corresponding current wave, Total harmonic distortion (THD) [11]. Asymmetrical multilevel inverter with 1:3 voltage propagation is developed, the Switching pulse for Asymmetrical multilevel inverter are generated using embedded controller with less number of switches and voltage sources compare to conventional multilevel inverters [12]. A comparison of sinusoidal and trapezoidal PWM strategies applied to a trinary DC source nine level inverter fed R – load with PI control scheme with sudden load changes at specified reference speed. [13]. A dc to dc converter topology is developed for the solar PV system to harvest the solar energy in efficient manner [14]. A new symmetric multilevel inverter topology is designed with lesser components compared to conventional multilevel inverters [15].

Hence, this study is focused on designing of non modular with asymmetric voltage ratio by making a trade-off between, the number of switches, voltage levels, and system structure complexity. In this work, 51-level circuit topology is proposed to produce all voltage levels with uniform step size utilizing fewer power switches. The proposed inverter is designed using MATLAB/Simulink software with simulations and verified by experimental results at restive and inductive load. The presented topology is also compared with traditional MLIs and other recently introduced MLIs to show its performance. Its structure and operating principle are addressed in Section II. In section III , the simulation and hardware results for 51 level non modular design are presented. Finally, the conclusion is presented in Section IV.

II. PROPOSED TOPOLOGY

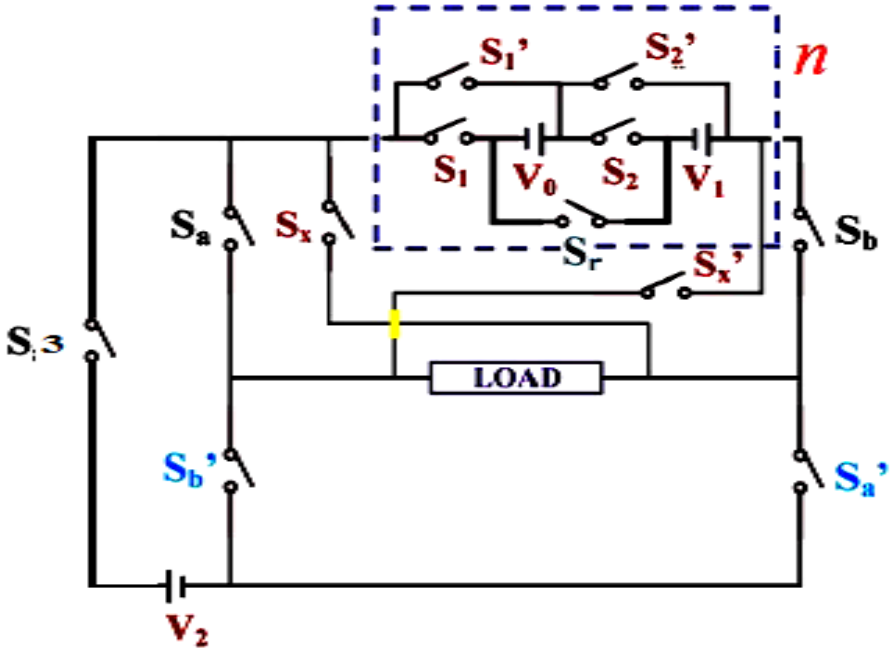

Figure 1: Schematic of Proposed Topology

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The basic skeleton of the proposed inverter circuit is shown in Fig.1. It consists of three separated dc sources (SDCs) with ten unidirectional and one bi-directional power switches. The unidirectional switch is power MOSFET with anti-parallel diode. The bidirectional power switch comprises two power MOSFETs, two anti-parallel diodes, and only one gate-driver circuits. The anti-parallel diodes are used to pass current in both directions, and voltage can be blocked in one direction only. The magnitudes of the SDCs are selected as V0 = 43V. V1=V2= 129 V. The module performs additive/subtractive function with the voltage sources (V2-Vn) when magnitudes of voltage sources are not equal. The conventional H-bridge with cross link connection in the upper half is named as HX bridge. The switches, S1 and S2, are complementary to the switch pair S1' and S2', which can connect/bypass the voltage sources, V0 and V1, while the switch Sr helps the voltage source (V1) to get subtracted from the V0. The tap switches, S3 to Sn11, link the separate DC sources of tapped sources stack to the load. The switches, Sx & Sx', and Sa, Sa', Sb and Sb' renders polarity reversal. The DC sources can be derived from DC-link capacitors or any other renewable energy sources. At m level, the proposed topology requires (n19) switches while the CHBMLI needs (4n), where, the separate DC source count is marked as "n". The suggested topology uses minimum switch count in the conduction loop to acquire various levels in the output voltage. The structure can be configured to produce different varieties of voltage levels with possible values of V0.

Table 1 shows the switching states of 17-level MLI.

The table 1, shows the switching pattern and the separated dc source voltage, for easy understanding the V0, V1 and V_2 are take as 1: 3: 3 Volts, such as V1 = 49 volts, and V2 = V3 = 129 volts at this asymmetric voltage ratio the non modular it can able to produce 51 voltage levels.

S1	S2	S3	S1'	S2'	Sa	Sb	Sa'	Sb'	Sx	Sx'	Sr	V_0	V_1	V_2	Mode
1	0	0	0	1	0	0	0	0	1	1	0	X	0	0	+V0
1	0	0	0	1	1	1	0	0	0	0	0	X	0	0	-V0
0	0	0	1	0	0	0	0	0	1	1	1	X	X	0	+(V1-V0)
0	0	0	1	0	1	1	0	0	0	0	1	X	X	0	-(V1-V0)
1	0	1	0	1	0	0	1	0	0	1	0	X	0	X	+(V2+V0)
1	0	1	0	1	0	1	0	1	0	0	0	X	0	X	-V2+V0)
1	1	0	0	0	0	0	0	0	1	1	0	X	X	0	+(V1+V0)
1	1	0	0	0	1	1	0	0	0	0	0	X	X	0	-(V1+V0)
0	1	1	1	0	0	0	1	0	0	1	0	0	X	X	+(V2+V1)
0	1	1	1	0	0	1	0	1	0	0	0	0	X	X	-(V2+V1)
0	0	1	1	0	0	0	1	0	0	1	1	X	X	X	+(V2-V0+V1)
0	0	1	1	0	0	1	0	1	0	0	1	X	X	X	-(V2-V0+V1)
1	1	1	0	0	0	0	1	0	0	1	0	X	X	X	+(V2+V0+V1)
1	1	1	0	0	0	1	0	1	0	0	0	X	X	X	-(V2+V0+V1)

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Table 2. Various parameters for proposed MLI topologies

The table 2, gives the clue to find parameters for proposed MLI topologies.

Parameters	Number of basic units	voltage level
Output Voltage level	(m+17)/2	51
Active switches	(m+17)/2	51
Gate drivers	12	51
Power diodes	13	51
Separated dc source	3	51

III. INVESTIGATION OF SIMULATION AND HARDWARE RESULT

For understanding the functioning of the suggested MLI in Modular with asymmetric modes, a detailed simulation study is carried out in MATLAB R2017b. The simulation parameters are as follows, V0=49 Volt, V1=V2= 149 Volt in the ratio of 1:3:3 to produce 300 V (peak) in the output voltage. Values of the RL load used in simulation study is R = 100 Ω and L = 100 mH. The switching frequency is 2 kHz. Fig.2 show s 51 level output voltage waveform with asymmetric voltage ratio of 1:3:3 Fig 3 shows output current waveform with asymmetric voltage ratio of 1:3:3. Fig. 4 charter output voltage spectra and inductive load current waveform for asymmetrical configuration obtained with 4.01% of THD. The simulation results evidence that the proposed topology is capable of giving high number of voltage levels with a minimum number of power components.

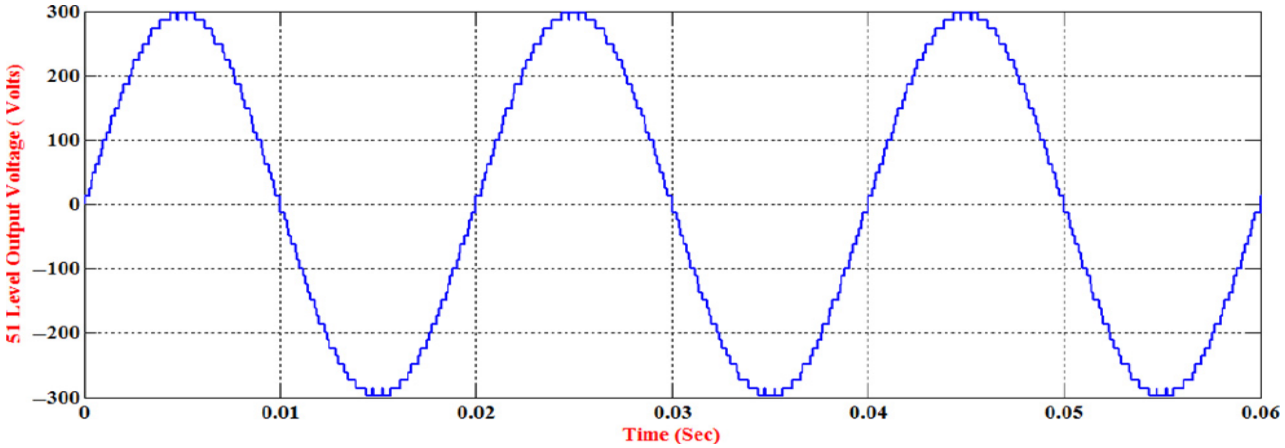

Figure 2: Simulation of 51 level output voltage waveform with asymmetric voltage ratio of 1:3:3

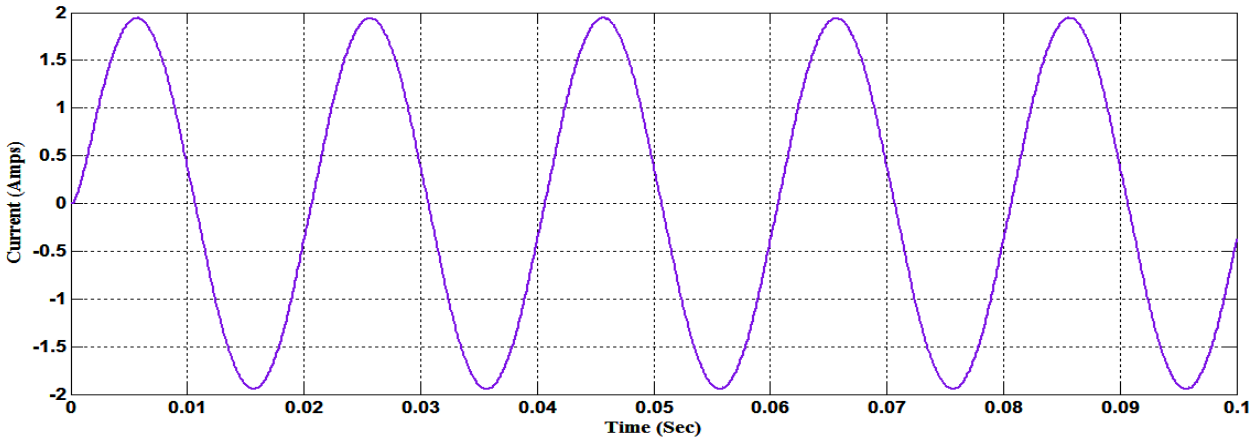

Figure 3: Simulation of Output current waveform with asymmetric voltage ratio of 1:3:3

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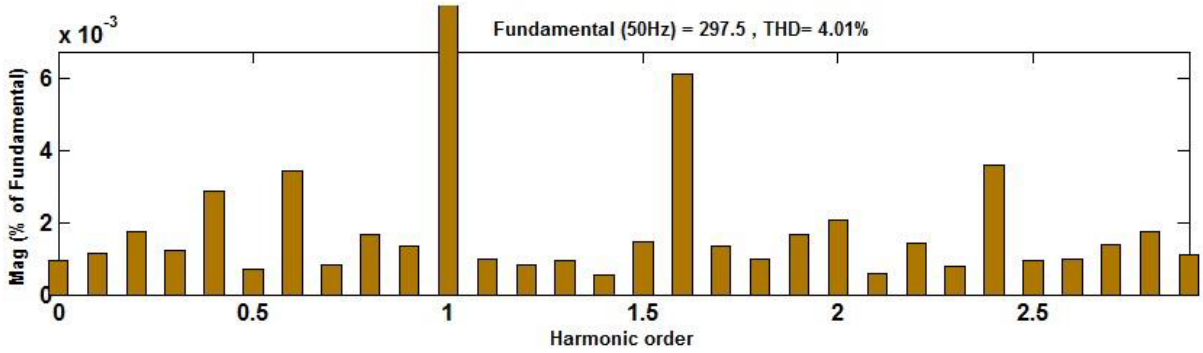

Figure 4: Harmonic spectrum of output voltage asymmetric voltage ratio of 1:3:3

Fig.5 show hardware results of s 51 level output voltage waveform with asymmetric voltage ratio of 1:3:3 Fig 6 show hardware results of output current waveform with asymmetric voltage ratio of 1:3:3. Fig. 7 shows hardware results of output voltage spectra and inductive load current waveform for asymmetrical configuration obtained with 3.52% of THD.

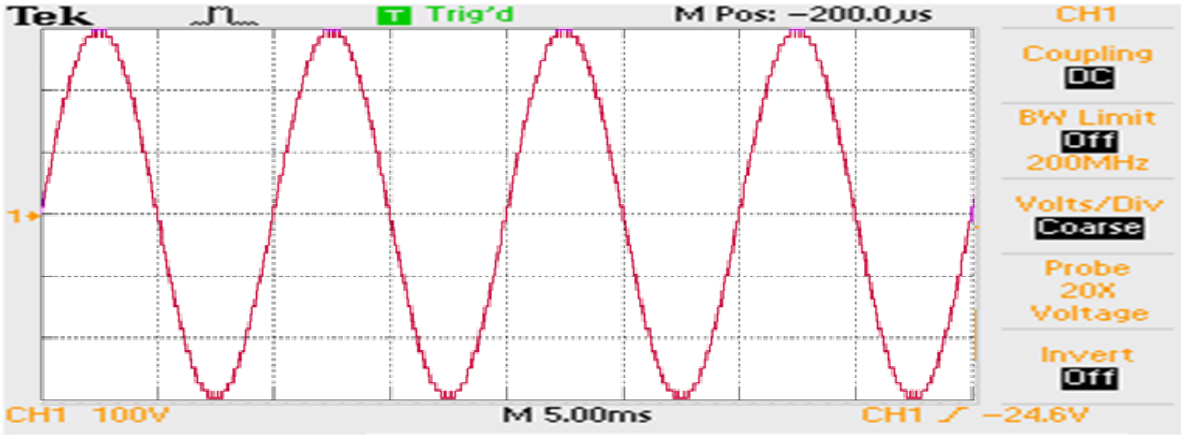

Figure 5: Hardware results of 51 level output voltage waveform with asymmetric voltage ratio of 1:3:3

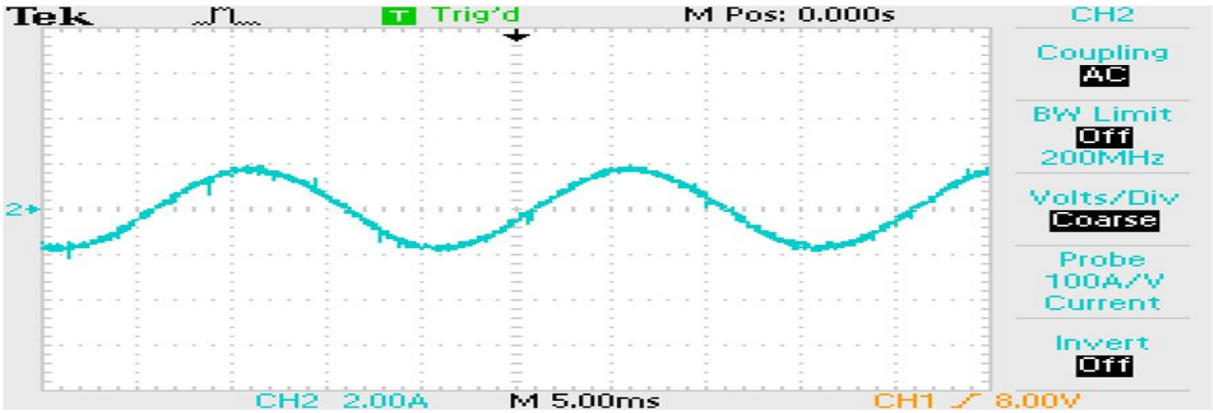

Figure 6: Hardware results of Output current waveform with asymmetric voltage ratio of 1:3:3

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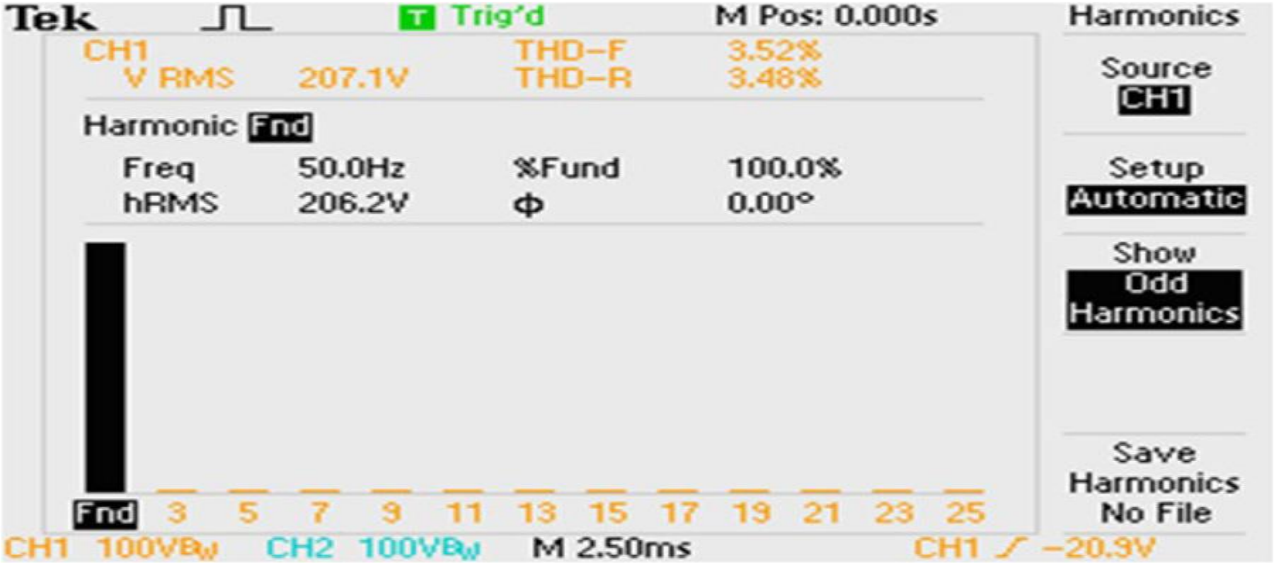

Figure 7: Hardware result of Harmonic spectrum of output voltage asymmetric voltage ratio of 1:3:3

IV. CONCLUSION

This research work proposed 51 level non modular MLI topology. The objective of the proposed MLI is to uses reduced number of power electronics components to produce higher voltage levels with low voltage rated power switches. The topology can generate fifty one voltage levels under non modular asymmetric source configuration. The inverter topology can be connected in cascade to increase voltage steps with lower power components and lower voltage stress on power components. The proposed inverter's main feature is that it can generate all voltage steps without utilizing an H-bridge inverter. Therefore, it is suitable for medium voltage and high voltage applications. Simulation results validate the feasibility of the proposed MLI circuit.

REFERENCE

1. *S.Jeevananthan, S.Paramasivam and S.Thamizharasan, (2012) "A novel invariable carrier frequency multi-level inverter PWM for balancing switching transitions and better distribution of harmonic power", Int. J. Power Electronics, Vol.4, No.3, pp.290-301.*
2. *Ebrahim Babaei, ConcettinaBuccella and Carlo Cecati, (2019) "New 8-Level Basic Structure for Cascaded Multilevel Inverters with Reduced Number of Switches and DC Voltage Sources", Journal of Circuits, Systems and Computers, Vol. 28, NO. 03*
3. *Babaei, E., Laali, S. and Bayat, Z. (2015), "A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches", IEEE Transactions on Industrial Electronics, Vol. 62 No. 2, pp. 922-929*
4. *Kannan C, Nalin Kant Mohanty, Selvarasu Ranganathan, "A New tapped sources stack succord modified HX Bridge MLI," Circuit World, Vol. 47 No. 2, pp. 164-172. https://doi.org/10.1108/CW-11-2019-0185.2020.*
5. *Nalin Kant Mohanty, Chandrasekaran, (2020) "A Flexible Rung Ladder Structured Multilevel Inverter" Tehnički vjesnik, Vol 27.No 4, pp 1044-1049. https://doi.org/10.17559/TV-20190427204209.2020.*
6. *S. S. Lee, (2018)"Single-Stage Switched-Capacitor Module (S3CM) Topology for Cascaded Multilevel Inverter," in IEEE Transactions on Power Electronics, vol. 33, no. 10, pp. 8204-8207.*
7. *S. Edwin Jose and S. Titus, (2016) "A level Dependent Sources Concoction Multilevel Inverter Topology with Reduced Number of Power" Journal of Power Electronics, Vol. 16, No. 4, pp. 1316-1323.*
8. *C.Kannan & Nalin Kant Mohanty "A Non-modular Matrix Structure for Component Count Waning in Multilevel Inversion" in Springer Journal of Electrical Engineering & Technology .2021. https://doi.org/10.1007/s42835-021-00916-0.*
9. *C.Kannan, Selvarasu, R. "Modelling and Control of Cascaded Multilevel Inverter for Harmonics Mitigation of Induction Motor Drive" in Springer Lecture notes during 2022 https://doi.org/10.1007/978-981-16-4943-1_5.*
10. *Kannan, C., Mohanty, N. K., & Selvarasu, R. "A new topology for cascaded H-bridge multilevel inverter with PI and Fuzzy control". Energy Procedia, 117, 917-926. https://doi.org/10.17559/TV-20190427204209.*
11. *Kannan Chandrasekaran, Nalin Kant Mohanty, Ashwin Kumar Sahoo "Performance Analysis Of Modular Vs Non Modular Multilevel Inverter" International Conference on Renewable Energy Integration into Smart Grids: IEEE, Xplore pp.61-67. https://doi.org/10.1109/ICREISG49226.2020.9174211.2020.*

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EPRA International Journal of Research and Development (IJRD)
Volume: 7 | Issue: 6 | June 2022 - Peer Reviewed Journal

12. Arun, V., and N. Prabaharan. "Micro controller based asymmetrical multilevel inverter." IAES International Journal of Robotics and Automation 8.1 (2019): 18. DOI: 10.11591/ijra.v8i1.pp18-25.
13. Arun, V., Prabaharan, N.(2019). "Induction motor drive with trinary dc source asymmetrical inverter", International Journal of Recent Technology and Engineering, 2019, Vol. 8, No.2, pp. 5484–5490. DOI: 10.35940/ijrte.B2527.078219.
14. Arun, V., Kumaraswamy, I., "DC-DC Converters in Solar PV System", International Journal of Innovative Technology and Exploring Engineering, 2020, Vol. 9, No.3, pp. 1693–1699, 2020. DOI: 10.35940/ijitee.B7037.019320.
15. Arun, V., Kumaraswamy, I., & Prabaharan, N. (2020). "Design and Realization of New structures of Multilevel Inverter for Seven Level Output Voltage", Solid State Technology, 63(5), 7392-7405.